Lifting Based 2D DWT Architecture for JPEG 2000

Jitendra Kumar Singh, Rakesh Patel, Ashish Singhadia

Abstract— In this thesis work, study and simulation has been carried out of a memory-efficient pipeline architecture which performs the two-dimensional discrete wavelet transform. Normally the memory size used by two-dimensional architecture mostly depends on the pipeline registers of (1-D) DWT. In this project work, the data path can be reduced with the help of the lifting-based DWT algorithm and high performance pipeline architecture. Efficient pipeline architecture and efficient multiplier can enhance performance and speed of processing of 2D DWT architecture for jpeg 2000 as compare to any other low performance direct implemented pipeline architectures. The merits of the lifting based DWT techniques is to divide into low pass and the high pass filters into a sequence of lower and upper triangular matrices. The given 2-D DWT architecture is composition of two 1-D processors (column-wise, row wise). Finally, the given architecture (2-D DWT architecture) implements both 9/7and 5/3 filters with the help of cascade the three key components. In this work, 12 bit floating point multiplier and a Baugh Wooley multiplier is simulated, which require less memory and do the fast multiplication. By replacing the 1D DWT architecture's multiplier with this multiplier a less memory and a lower delay 1D DWTarchitecture can be obtained.
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Index Terms— 2-D (two-dimensional), CSA (Carry Save Adder tree), DWT(Discrete Wavelet Transform, IO(input, output) , JPEG (Joint Photographic Experts Group), RAM(Random Access Memory), RPA (recursive pyramid algorithm) .

1 INTRODUCTION

The two-dimensional Discrete Wavelet Transform (DWT) has been very useful and applied in mostly image compression techniques. The Discrete Wavelet Transform (DWT) is being mostly used for image coding process. This is because of that DWT supports features like by resolution, region of interest coding, progressive image transmission by quality ease of compressed image manipulation, etc. One major drawback of the conventional convolution based Discrete Wavelet Transform DWT is, it requires a lot of computations.The wavelet transform decompose the signals into different different sub-bands and produces both time and frequency information which supports methods for analysing various signals. Many areas such as image analysis, digital signal processing and communication used DWT techniques. the demand for heavy internal memory requirements and real-time performance are the main issues for hardware implementation . The 2-D DWT can generally realized by separable approach, which splits the 2-D DWT implementation into two 1D operations (columnwise and rowwise filtering)and non-separable approach .From 1990 to 2014 there are number of research work carried out in this area. K.K.Parthi and T.Nishantani present a combined (folded) architecture and digital-serial architecture to minimize the register and latency [5]. M.Vishwanath design a systolic parallel architecture to perform the recursive pyramid algorithm (RPA) with less storage and short latency [14].

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A less computationally intensive lifting-based DWT architecture [2] is used to carry out the bi orthogonal wavelet filtering. The computational complexity can be reduced effectively by the factorizing conventional filter banks into many lifting steps. The memory prerequisite of lifting-based DWT [[1]] can also be reduce as compare to the convolutional DWT, based on the line-based architecture [[5]].The lifting scheme involves lower memory and less computation, the irregular and longer data paths are the main limitations for efficiency of hardware implementation.

The lifting based scheme for the 2D-DWT helps in overcome drawback and has been chosen in the JPEG2000 standard. JPEG 2000 [[6]] is the coding system and an image compression standard and it was created by the committee of Joint Photographic Experts Group in 2000, with a newly designed, wavelet-based methodology. With the help of advance, fast and less memory required multiplier, speed of operation can be increases which require less memory space. The Baugh-Wooley multiplication algorithm has been developed in order to design regular multiplier which is an efficient way to handle the sign bits. This technique, suited for 2's-compliment number. Baugh-Wooley multiplier is the paramount known algorithm (for signed multiplication) which is Two's compliment Signed multipliers , because it permit all the partial products to have positive signbits and maximizes the regularity of the multiplier.

The rest of this paper organised as follow. Section briefly introduces Lifting-Based and modified Lifting-Based Discrete Wavelet Transform. Third section introduces Baugh-Wooley multiplier which is main focused area in this paper. In fourth section Experiment and Result. In fifth section conclusion. Experimental results demonstrate that the Baugh Wooley Multiplier circuit improves the accurate performance, reduces the complexity of hardware and also reduces power consumption.

2 PROPOSED METHODOLOGY

a-Primitive Lifting-Based *DWT*-

The lifting-based DWT is first derived by Daubechies and Sweldens [7]. The lifting scheme, splits DWT filter bank into many lifting steps. Fig 1 shows a block diagram of the lifting-based structure. The g (z) and h (z) are the high-pass and low-pass analysis filters. The poly-phase matrix $\tilde{p}(z)$ is defined by this equation:

$$\tilde{p}(z)= \begin{bmatrix} \tilde{h}_e(z) & \tilde{h}_o(z) \\ \tilde{g}_e(z) & \tilde{g}_o(z) \end{bmatrix} \quad \text{.....(1)}$$

The polyphase matrix $\tilde{p}(z)$ can be factorized into a constant diagonal matrix of the primitive lifting-based structure multiplied by a sequence of alternat lower and upper triangular matrices.

$$\tilde{p}(z) = \begin{pmatrix} K_1 & 0 \\ 0 & K_2 \end{pmatrix} \prod_{i=1}^{m} \left\{ \begin{pmatrix} 1 & 0 \\ \tilde{t}_1(z) & 1 \end{pmatrix} \begin{pmatrix} 1 & \tilde{s}_1(z) \\ 0 & 1 \end{pmatrix} \right\} \quad \text{……..2}$$

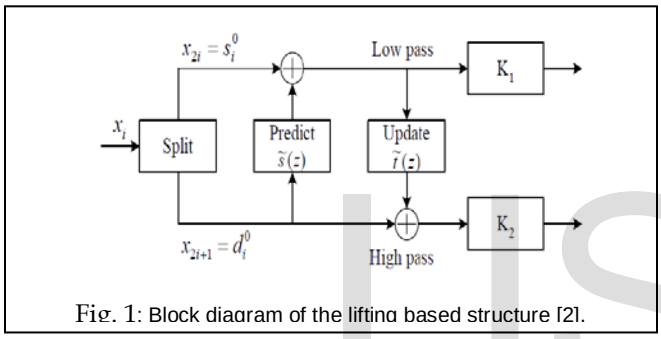

Fig. 1: Block diagram of the lifting based structure [2].

Where K1 and K2 are the scaling factors, and s (z) and p (z) are the prediction and update operators respectively and n is the lifting step. The 9/7 filter has one scaling step and two lifting steps while the 5/3 filter can be regarded as aspecial case with single lifting step. The detailed forward algorithm of the 9/7 filter is described by wavelet coefficients si(low-pass coefficients) and di(high-pass coefficients) can be obtained.

(i) Splitting Step:

$$d_i^0 = x_{2i+1} \quad (3)$$

$$s_i^0 = x_{2i} \quad (4)$$

(ii) Lifting Step:

(First) $d_i^1 = d_i^0 + \alpha \times (s_i^0 + s_{i+1}^0)$. (Predictor) (5)

$$s_i^1 = s_i^0 + \beta \times (d_{i-1}^0 + d_i^0). \quad \text{(Updater)} \quad (6)$$

(Second) $d_i^2 = d_i^1 + \gamma \times (s_i^1 + s_{i+1}^1)$. (Predictor) (7)

$$s_i^2 = s_i^1 + \delta \times (d_{i-1}^1 + d_i^1) \text{ (Updater)} \quad (8)$$

(iii) Scaling Step:

$$d_i = K_1 \times d_i^2 \quad (9)$$

$$s_i = K_1 \times s_i^2 \quad (10)$$

Several architectures have been projected to implement the lifting structures of the 5/3 and 9/7 filters. Fig. 2 depicts the 1-D lifting-based, direct mapping hardware architecture [2] for the 1-D lifting-based DWT. The required four stages of pipeline used to reduces the processing time, but the vital path is still limited by the computation of predictor or updater. Which are two adders and one multiplier propagation delay. Moreover, it require 32 pipeline registers to reduce the critical path to one multiplier delay.

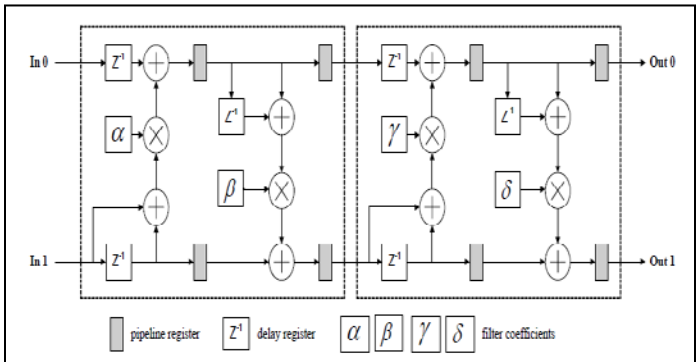

Fig. 2: the 1-D lifting-based DWT- Ddirect mapping hardware architecture [2]

b- Modified Lifting-Based Discrete Wavelet Transform

Since the predictor or updater reduces the critical timing delay, we combine the predictor and updater stages in a single lifting step. By combine (5) into (6), the lifting step will be expressed as one equation and each operation is performed by multiplication or addition as follows:

$$s_i^1 = s_i^0 + \beta \times \{[d_{i-1}^0 + \alpha \times (s_{i-1}^0 + s_i^0)] + [d_{i-1}^0 + \alpha \times (s_i^0 + s_{i+1}^0)]\}.$$

$$s_i^1 = s_i^0 + (\beta \times d_{i-1}^0 + \beta\alpha\, s_{i-1}^0 + \beta\alpha s_i^0) + (\beta d_{i-1}^0 + \beta\, \alpha s_i^0 + \beta\alpha s_{i+1}^0).$$

……(11)

In the second lifting step, Eq. (7) substitutes into Eq. (8) as the first lifting step. While the outputs of the first step of lifting are s_i^1 and βd_i^1 a factor β is derived to let the output βd_i^1 from the first lifting step can be obtained directly. In this adjustment, Eq. (11) has the same form as Eq. (12), which indicates that the two lifting steps can be realized in the same architecture. The second lifting step equations are written as follows:

$$s_i^2 = s_i^1 + \delta \times (d_{i-1}^0 + d_i^0).$$

$$s_i^2 = s_i^1 + \delta \times \{[d_{i-1}^1 + \gamma \times (s_{i-1}^1 + s_i^1)] + [d_i^1 + \gamma \times (s_i^1 + s_{i+1}^1)]\}.$$

$$s_i^2 = s_i^1 + (\tfrac{\omega}{n} \times \beta d_{i-1}^1 + \delta\gamma \times s_{i-1}^1 + \delta\gamma s_i^1) + (\tfrac{\omega}{n} \times \beta d_i^1 + \delta\gamma \times s_i^1 + \delta\gamma \times s_{i+1}^1).$$

$$s_i^2 = s_i^1 + (\tfrac{\omega}{n} \times \beta d_{i-1}^1 + \delta\gamma \times s_{i-1}^1 + \delta\gamma s_i^1) + (\tfrac{\omega}{n} \times \beta d_i^1 + \delta\gamma \times s_i^1 + \delta\gamma \times s_{i+1}^1). \quad (12)$$

The scaling step is finally represented as follows:

$$d_i = \tfrac{n_2}{\omega} \times (\delta d_i^2) \quad (13)$$

$$s_i = K_1 \times s_i^2 \quad (14)$$

The above equations need six multipliers coefficient β, βα, $\frac{\omega}{n}$, δγ, $\frac{n_2}{\omega}$, K_1 to perform the lifting and scaling steps. The primitive and modified algorithms have the equal number of multipliers. Moreover, the modified algorithm provides the lengthy computation data path of both the predictor and updater such that the arithmetic property can be performed and used some more efficiently. The inverse transform may be modified in the similar manner as the other case like forward case. The inverse transform begin from the

scaling step.

$$s_i^2 = K_1^{-1} \times s_i \quad (15)$$

$$d_i^2 = K_2^{-1} \times d_i \quad (16)$$

The predictor and updater can be combined into a single equation, as shown in Eq. (3.17). By substituting $s_i^2 = K_1^{-1} \times s_i$ into the s_i^2 term, a new multiplier term, γK^{-1} is derived. It also reduces one multiplication operation for the input sequence s_i.

$$d_i^1 = d_i^2 - \gamma \times (s_i^1 + s_{i+1}^1).$$

$$d_i^1 = d_i^2 - \gamma \times \{[s_i^2 - \delta \times (d_{i-1}^2 + d_i^2)] + [s_{i+1}^2 - \delta \times (d_i^2 + d_{i+1}^2)]\}.$$

$$d_i^1 = d_i^2 - (\gamma K_1^{-1} \times s_i - \gamma\delta \times d_{i-1}^2 + \gamma\delta \times d_i^2) - (\gamma K_1^{-1} \times s_{i+1} - \gamma\delta \times d_i^2 + \gamma\delta \times d_{i+1}^2). \quad (17)$$

Similarly, a factor γ is derived such that d_i^1, γs_i^1 can be get directly. The equations are rewritten as follows:

$$d_i^0 = d_i^1 - \alpha \times (s_i^0 + s_{i+1}^0). \quad (18)$$

$$d_i^0 = d_i^1 - \alpha \times \{[s_i^1 - \beta \times (d_{i-1}^1 + d_i^1)] + [s_{i+1}^1 - \beta \times (d_i^1 + d_{i+1}^1)]\}.$$

$$d_i^0 = d_i^1 - \frac{\alpha}{\gamma} \times \{[\gamma s_i^1 - \gamma\beta \times (d_{i-1}^1 + d_i^1)] + [\gamma s_{i+1}^1 - \gamma\beta \times (d_i^1 + d_{i+1}^1)]\}.$$

$$d_i^0 = d_i^1 - (\frac{\alpha}{\gamma} \times \gamma s_i^1 - \alpha\beta \times d_{i-1}^1 - \alpha\beta \times d_i^1)] - (\frac{\alpha}{\gamma} \times \gamma s_{i+1}^1 - \alpha\beta \times d_i^1 - \alpha\beta \times d_{i+1}^1). \quad (19)$$

TABLE 1

Coefficients Represented in the Binary Forms(the 9/7 Filter)

FORWARD COEFFICIENTS			INVERSE COEFFICIENTS		
Coefficients	Value	Absolute value by 12 bits	Coefficients	Value	Absolute value by 12 bits
Bα	0.083984375	.000101011000	γK_1^{-1}	0.54296875	.100010110000
(δ/β)>>1	-4.1855446875	100.001011111	$(\delta\gamma)_{\gg 1}$	0.195556640625	.001100100001
(δγ)>>1	0.195556640625	.001100100001	$(\alpha/\gamma)_{\gg 1}$	-.898193359375	.111001011111
(K2/δ)>>1	5.546875	101.100011000	$(\beta\alpha)_{\gg 1}$	0.0419921875	.000010101100
(K_1)<<1	1.62548828125	1.101000000001	$(\alpha^{-1})_{\ll 2}$	-2.521484375	10.100001 0110

Finally, to reconstruct the even part of the data, the coefficient α^{-1} is applied to bring back the output s_i^0

$$s_i^0 = \alpha^{-1} \times s_i^0 \quad (20)$$

Both modified and primitive IDWT algorithms have constant six multipliers. In the modified case, the six constant multipliers are K_2^{-1}, γK_1^{-1}, $\gamma\delta$, $\frac{\alpha}{\gamma}$, $\alpha\beta$, and α^{-1}. To avoid the instance of run over, the huge absolute coefficients, $\gamma\delta$ and $^{\delta}/_{\beta}$, can be further scaled. In TABLE 1 coefficients in binary form of forward and inverse transform is shown. Although larger scaling factors can decrease the overflow instances, the overall finite word length precision would be decreased significantly. The quality values of coefficients are depending on both the 8-bit raw data and 12-bit data coefficients specified in TABLE 1.

C- 2D DWT Overall Architecture

The given architecture performs the forward and inverse 2-D DWT transform in the column-row fashion. Fig. 3 depicts the overall 2-D DWT architecture, which includes three main components — the column processor, the transposing buffer and the row processor. To carry out the one-level decomposition for an NxM image, the given architecture executes the column processor, the transposing buffer and the row processor simultaneously, where N and M represent the image height and width. Moreover, the row processor has to execute row-wise transform once enough column processed data are obtained to decrease the internal memory size. Thereafter, the MN/4size external RAM is used to store the LL band output coefficients for the next level decomposition.

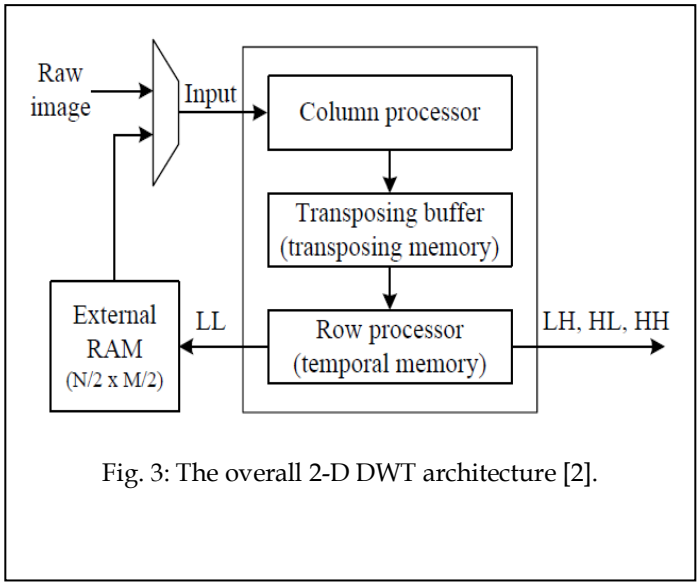

Fig. 3: The overall 2-D DWT architecture [2].

D - Baugh Wooley Multiplier

Baugh-Wooley is Two's compliment Signed multipliers, which is the best known multiplier algorithm for signed mul-

tiplication as it maximizes the reliability of the multiplier and allow all of the partial products tp provide positive sign bits and it avoid having deal with the negatively weighted bits .The Baugh–Wooley multiplication algorithm which was developed to design for Two's compliment number's direct multipliers .When two's compliment numbers direct multiplying, each of the partial products of multiplication to be added is a signed numbers. Therefore each partial product must be sign (for signed multiplication) extended to the width of the final product in order to structure a correct sum by the Adder CSA(Carry Save Adder tree). According to efficient method Baugh-Wooley approach, of count additional entries to the bit matrix recommended to keep away from using with the negatively weighted bits in the partial product matrix for multiplication.

In fig 4 is partial product arrays of 5*5 bits Unsigned & fig 5 is partial product arrays of 5*5 bits Signed bits are shown:

					a_4	a_3	a_2	a_1	a_0
					x_4	x_3	x_2	x_1	x_0
					a_4x_0	a_3x_0	a_2x_0	a_1x_0	a_0x_0
				a_4x_1	a_3x_1	a_2x_1	a_1x_1	a_0x_1	
			a_4x_2	a_3x_2	a_2x_2	a_1x_2	a_0x_2		
		a_4x_3	a_3x_3	a_2x_3	a_1x_3	a_0x_3			
	a_4x_4	a_3x_4	a_2x_4	a_1x_4	a_0x_4				
p_9	p_8	p_7	p_6	p_5	p_4	p_3	p_2	p_1	p_0

Fig. 4; 5*5 unsigned multiplications [12]

					a_4	a_3	a_2	a_1	a_0
					x_4	x_3	x_2	x_1	x_0
					$-a_4x_0$	a_3x_0	a_2x_0	a_1x_0	a_0x_0
				$-a_4x_1$	a_3x_1	a_2x_1	a_1x_1	a_0x_1	
			$-a_4x_2$	a_3x_2	a_2x_2	a_1x_2	a_0x_2		
		$-a_4x_3$	a_3x_3	a_2x_3	a_1x_3	a_0x_3			
	a_4x_4	$-a_3x_4$	$-a_2x_4$	$-a_1x_4$	$-a_0x_4$				
p_9	p_8	p_7	p_6	p_5	p_4	p_3	p_2	p_1	p_0

Fig. 5: 5*5 signed multiplications [12]

Experimental result demonstrate that the Baugh Wooley Multiplier circuit improves the accurate performance, reduces the complexity of hardware and also reduces power consumption that is dynamic power 15.3mW and the required maximum clock period of 3.912ns which is very efficient and reliable as compared to the reference paper

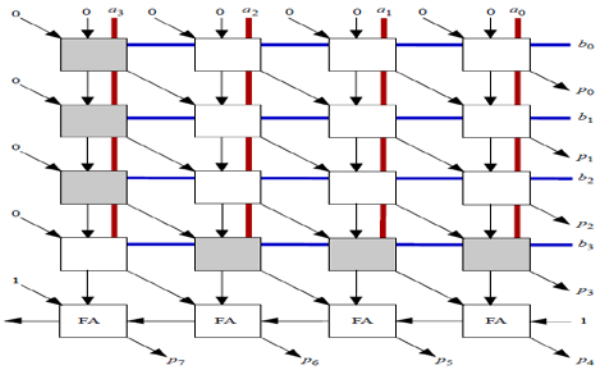

Fig. 6: Block diagram of 4 x 4 Baugh Wooley Multipli-

(a) Baugh-Wooley multiplier white-cell (b) Baugh-Wooley multiplier gray-cell

Fig. 7: Baugh Wooley Multiplier basic cell instruction

3 EXPERIMENT AND RESULT

This section deals with the simulation of Column Processor, Row Processor, Transposing Buffer, Floating Point Multiplier and Baugh Wooley Multiplier in XILINX ISE Simulator as well as in MATLAB showing the 2nd level decomposition of image on application of 2D- DWT. The overall time obtain by Baugh Wooley Multiplier

Is 197 ns and memory requirement 1674 KB, Normally other multiplier gets more than 500ns. This is much lesser than other multiplier. Experimental result demonstrate that the Baugh Wooley Multiplier circuit improves the accurate performance, reduces the complexity of hardware and also reduces power consumption that is dynamic power 15.3mW and the required maximum clock period of 3.912ns which is very efficient and reliable as compared to the reference paper.

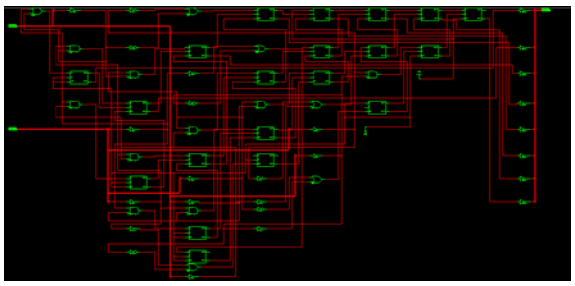

Fig. 8 : Technology Schematic of 4 Bit Baugh Wooley Multiplier in Xilinx

Simulation of Column Processor, Row Processor, Transposing Buffer, Floating Point Multiplier are easy to design in this thesis work our main focus on Baugh Wooley Multiplier which is shown in fig. 08 in XILINX ISE Simulator .

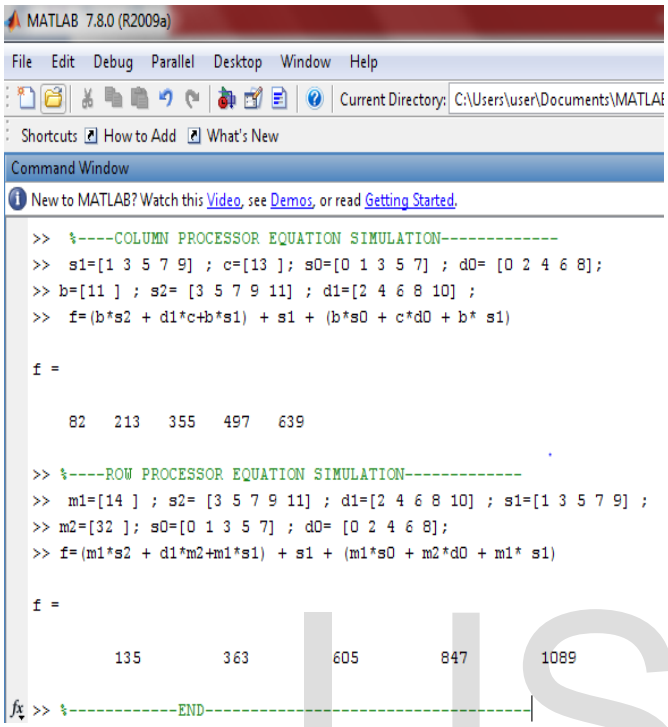

Fig.9: Result of CP and RP equation (12) simulation in MATLAB

(2) Simulation Results in MATLAB of 2D DWT of an image. Then in fig 11 shown the 4 different configuration of image LL,HL,LH and HH.

In fig 12 there is a compaision between original and compressed image. And fig 13 shows the DWT and inverse DWT of image.

Fig.109: Original image

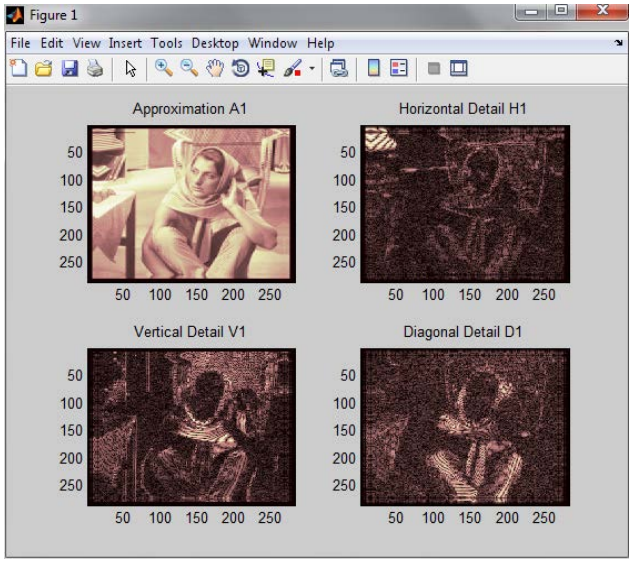

Fig. 11: Displaying the Approximation and Details of image

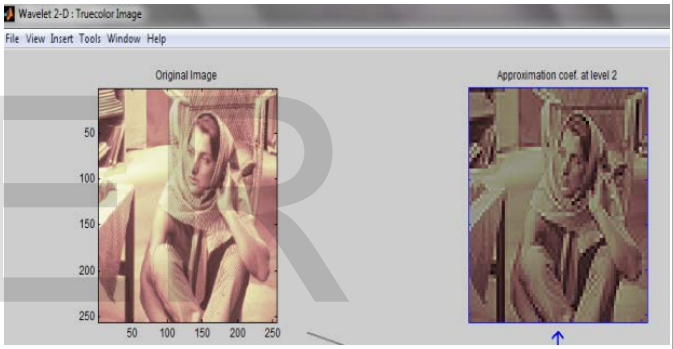

Fig. 12: Displaying the original and compressed image

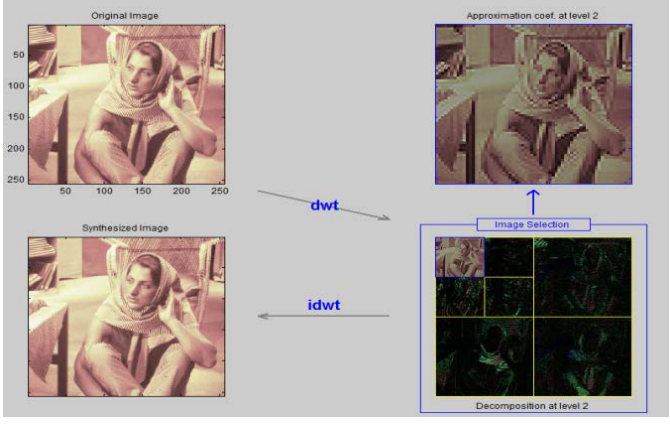

Fig. 13: Displaying the forward DWT and inverse DWT of image, using GUI in MATLAB

FPGA Requirement -

FPGA Requirement of Five Main Entities

ENTITY	CELLS USAGE		MEMORY USAGE	PROCESSING TIME TAKEN
	ELEMENTS	NO.S OF ELEMENT		
FLOATING POINT MULTIPLIER	BELs	706	170400 KB	250 ns
	FF/LD	54		
	IO BUFFERS	61		
COLUMN PROCESSOR	BELs	1463	178848 KB	410 ns
	FF/FD	168		
	IO BUFFERS	61		
	TRISTATE BUFFERS	48		
TRANSPOSING BUFFER	BELs	706	167000 KB	220 ns
	IO BUFFERS	73		
	TRISTATE BUFFERS	1		
ROW PROCESSOR	BELs	1463	178848 KB	410 ns
	FF/FD	168		
	IO BUFFERS	61		
	TRISTATE BUFFERS	48		
BAUGH WOOLEY MULTIPLIER	BELs	67	1674 KB	197 ns
	FF/FD	0		
	IO BUFFERS	16		
	TRISTATE BUFFERS	0		

4 . CONCLUSION

The Discrete Wavelet Transform provides a representation of signals with multi resolution. The transform can be implemented using filter banks. This report presents the simulation work for column processor, transposing buffer and row processor of 2D DWT architecture for JPEG 2000 and the study of high-performance and low-memory pipeline architecture for 2-D lifting-based DWT of the 5/3and 9/7 filters. By merging the predictor and updater into one single step, we can derive efficient pipeline architecture [2]. Hence, given the same number of arithmetic units, the given architecture has a shorter pipeline data path .In this thesis, architectures for the Lifting based DWT have been implemented. For each of them, parameters such as memory requirement and speed were discussed. The simulation results verify the functionality of the design. The proper scheduling of the wavelet coefficients to the Transposing Buffer ensures that, when the coefficients are finally read back from the Transposing Buffer, they are available in the required order for further processing by Row Processor. The proposed architecture [2] is simple since further levels of decomposition can be achieved using identical processing elements. The architecture provides parallel processing with fast computation of DWT . It has low memory requirements as compare to other and consumes very low power.

5. ACKNOWLEDGMENT

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